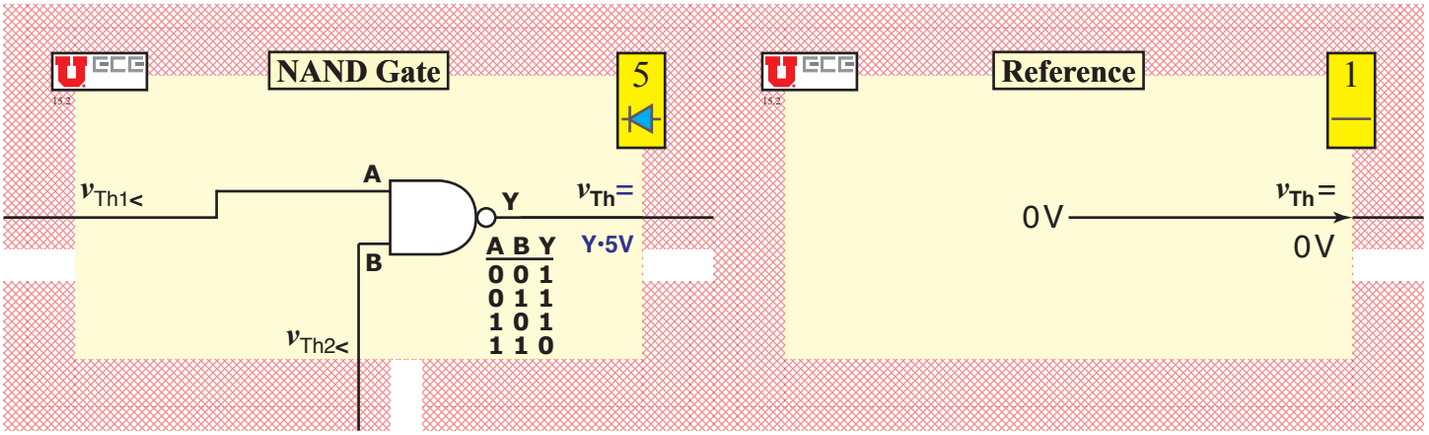
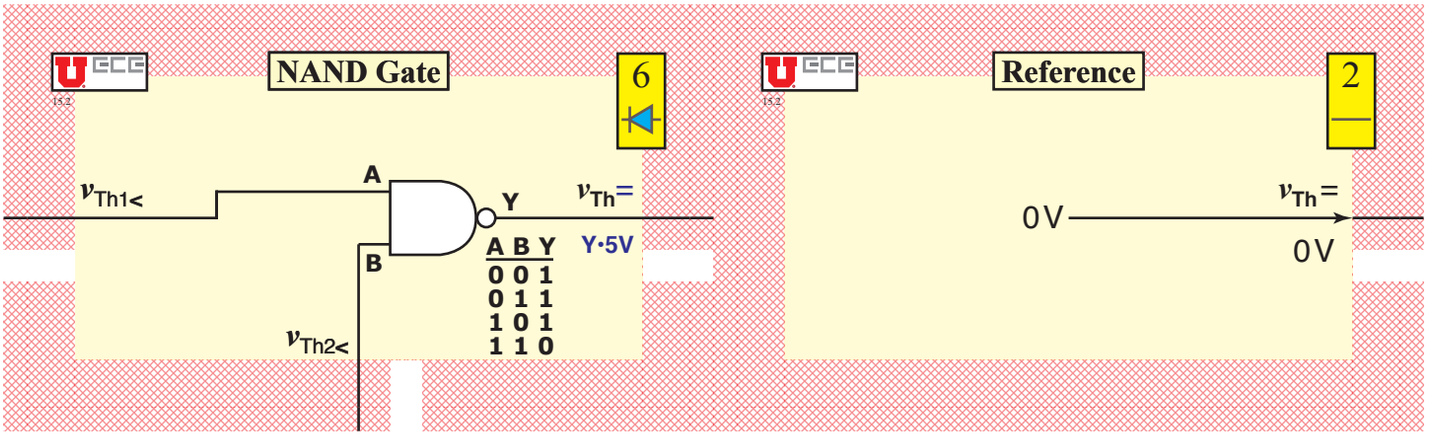
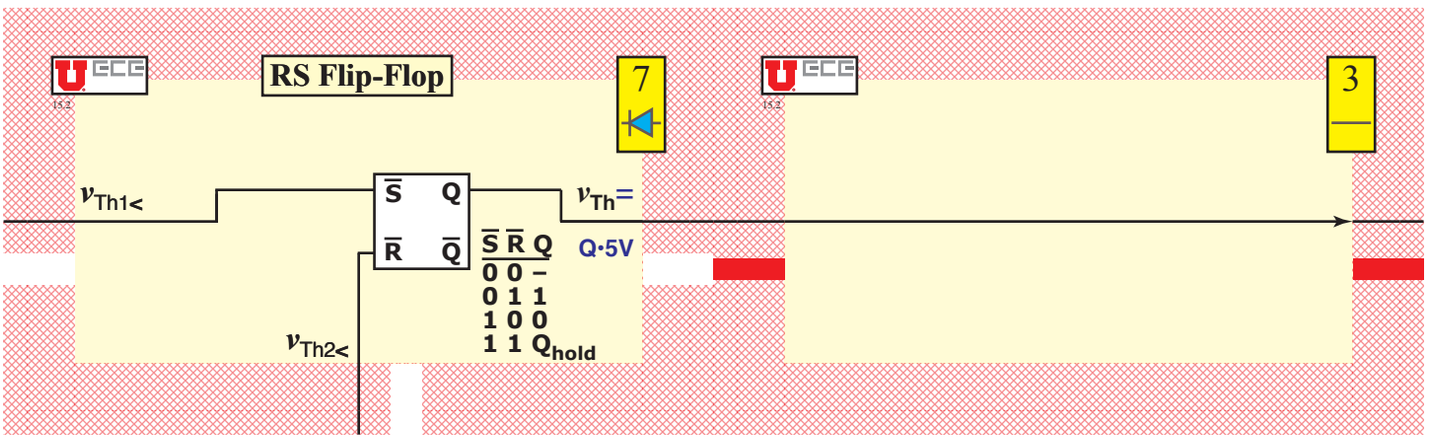

NAND Gate
5
$v_{Th1<}$
A
B
Y
$v_{Th2<}$
$v_{Th=}$
Y·5V
A B Y
0 0 1
0 1 1
1 0 1
1 1 0

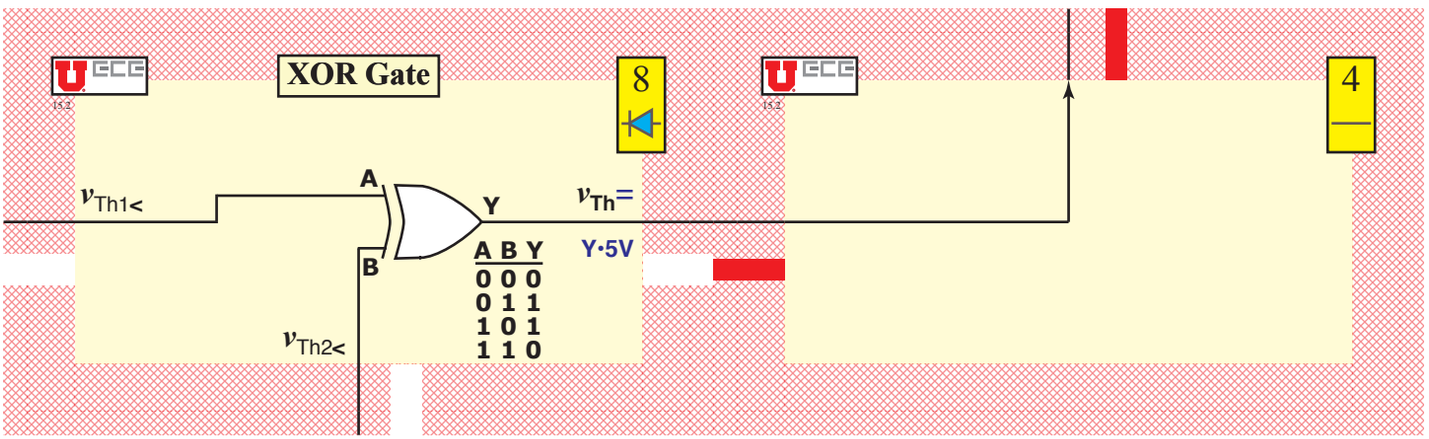

Reference
1
0V
$v_{Th=}$
0V

NAND Gate
6
$v_{Th1<}$
A
B
Y
$v_{Th2<}$
$v_{Th=}$
Y·5V
A B Y
0 0 1
0 1 1
1 0 1
1 1 0

Reference
2
0V
$v_{Th=}$
0V


RS Flip-Flop
7
$v_{Th1<}$
$\overline{S}$
Q
$\overline{R}$
$\overline{Q}$
$v_{Th2<}$
$v_{Th=}$
Q·5V
$\overline{S}$ $\overline{R}$ Q
0 0 –
0 1 1
1 0 0
1 1 Q_{hold}

3


XOR Gate
8
$v_{Th1<}$
A
B
Y
$v_{Th2<}$
$v_{Th=}$
Y·5V
A B Y
0 0 0
0 1 1
1 0 1
1 1 0

4