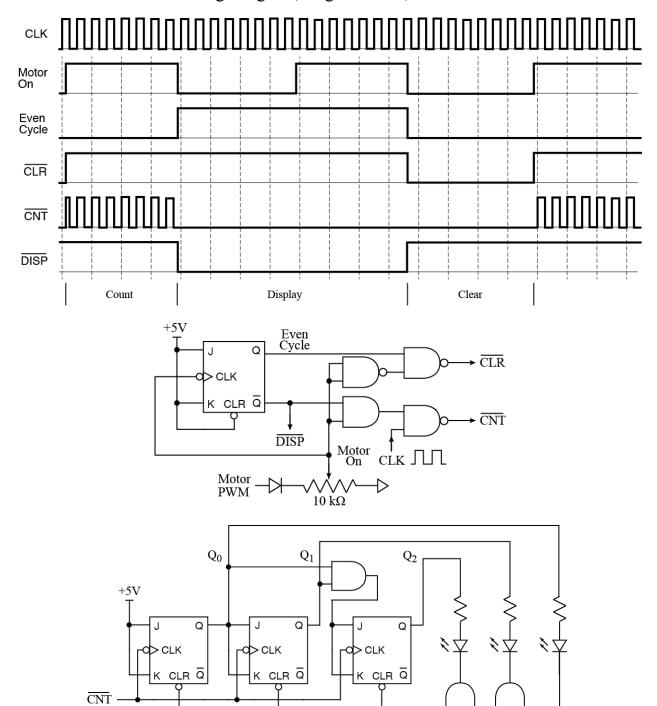
$\overline{\text{CLR}}$

Laboratory 7: Timing Diagram, Logic Circuit, and Counter



 $\overline{\text{DISP}}$