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TOOL: Steps to analyze an NMOS FET DC operating (or bias) point.

Check that source voltages are appropriate for FET to be active (on)

Set all coupling and bypass capacitors to be OPEN circuits

Set AC sources = 0V (not required if AC source isolated by C)

Use $I_G = 0\,\text{V}$ and $I_D = I_S$

Assume Saturation Mode (simplest case to analyze)

$$I_D = \frac{k_n}{2}(V_{GS} - V_{TH})^2 \qquad (1)$$

Use (1) as one equation for I_D and V_{GS}

If there is a current source in the FET source circuit,

Find V_{GS} using (1), and use steps below for ideas on how to solve for V_G and V_S

If the Gate is not connected to the drain or source in any way,

Find the node-voltage V_G from circuitry connected to gate

Write an equation for V_S in terms of I_D, V_{SS}, and resistance

Write an equation for V_{GS} as the V_G equation minus the V_S equation

Using (1) and the V_{GS} equation, solve for V_{GS} and I_D (the operating point)

If the Gate is connected to *only* the drain in some way,

Use $V_G = V_D$ (since current into gate is zero) to conclude that $V_{GS} = V_{DS}$

For a graphical solution: (also gives correct answer for triode mode)

Find points on the FET's characteristic curves where $V_{GS} = V_{DS}$, and use these points as a constraint curve in the solution for I_D

Write a load-line equation for I_D versus $V_{DS} = V_{GS}$ in terms of drain and source resistance, voltage and current sources, and I_D, and find the operating point as the intersection of the load-line and the curve for $V_{GS} = V_{DS}$ on the characteristic curves, or

For an algebraic solution:

Use $V_{GS} = V_{DS}$ as a constraint equation

Use algebra to solve for the intersection of the load-line equation and (1) with V_{DS} substituted for V_{GS}

If the Gate is connected to other things in a less common way,

Write $V_{GS} = V_G - V_S$, and use node-voltage analysis to write equations for all the circuit nodes (with (1) used as the quadratic value of the dependent source for I_D)

Check that the FET is in saturation: $V_{DS} > V_{GS} - V_{TH}$

If FET is not in saturation, **assume triode mode**

$$I_D = \frac{1}{2} k_n [2(V_{GS} - V_{TH}) V_{DS} - V_{DS}^2] \qquad (2)$$

For an algebraic solution:

Write $V_{GS} = V_G - V_S$ and $V_{DS} = V_D - V_S$, and use node-voltage analysis to write equations for all the circuit nodes (with (2) used as the nonlinear value of the dependent source for I_D)

For a graphical solution: (also gives correct answer for triode mode)

If the Gate is not connected to the drain or source in any way,

Find the node-voltage V_G from circuitry connected to gate

Write a load-line equation for I_D versus $V_{DS} = V_{GS}$ in terms of drain and source resistance, voltage and current sources, and I_D,

Draw the load-line on the characteristic curves as one constraint on the operating point

For several points on the load-line, determine V_{GS} and write the values at its point on the load-line

Determine which point on the load line has a V_{GS} value that matches that of a characteristic curve passing through it; this is the operating point