EX: Find the possible operating values vs v_{in} of the inverter in Fig. 1 with $V_{DD} = 6$V.

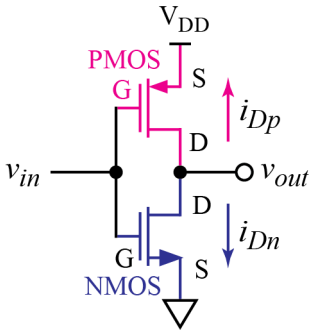
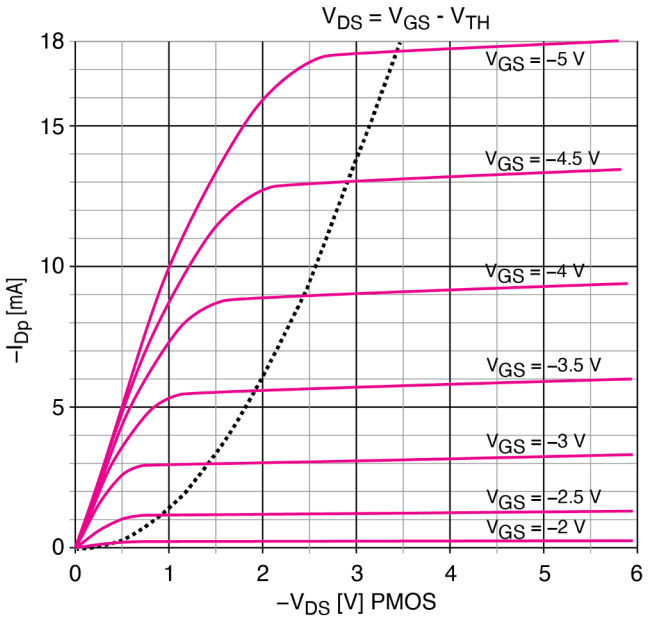


Fig. 1. Inverter schematic.

Fig. 2 shows characteristic curves of the PMOS transistor with the following parameters:

$V_{TH} = -1.6$ V

$k_p = 3.5$ mA



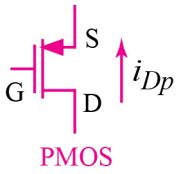


Fig. 2. PMOS characteristic curves.

Fig. 3 shows another way of viewing the PMOS characteristics that is convenient for analysis of the logic gate inverter.

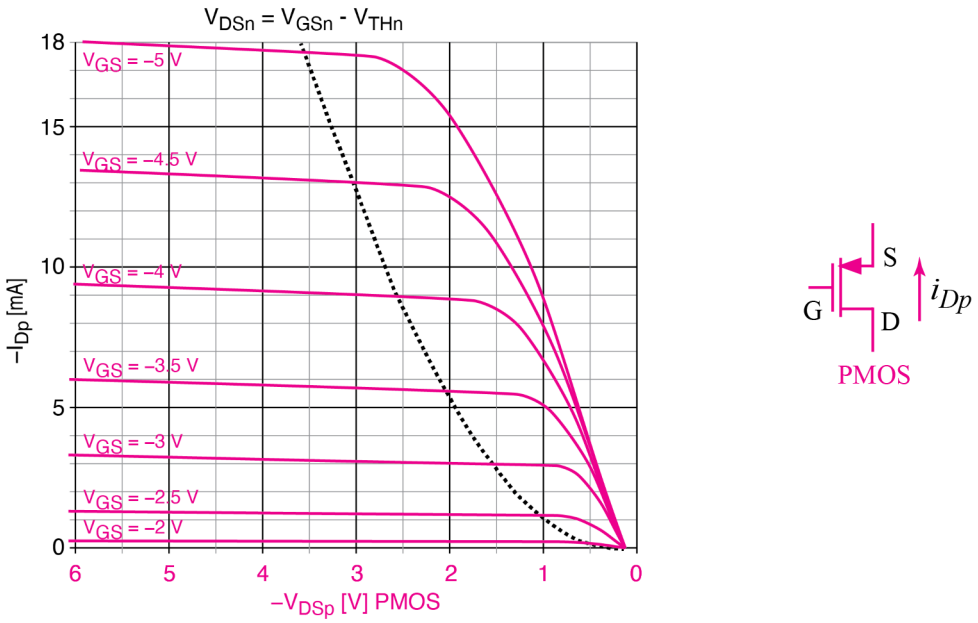


Fig. 3 PMOS characteristic curves redrawn

Fig. 4 shows the NMOS FET, which has the same parameters as the PMOS FET ($k_n = k_p$, etc.) but with the signs of I_D, V_{DS}, V_{GS}, and V_{TH} inverted.

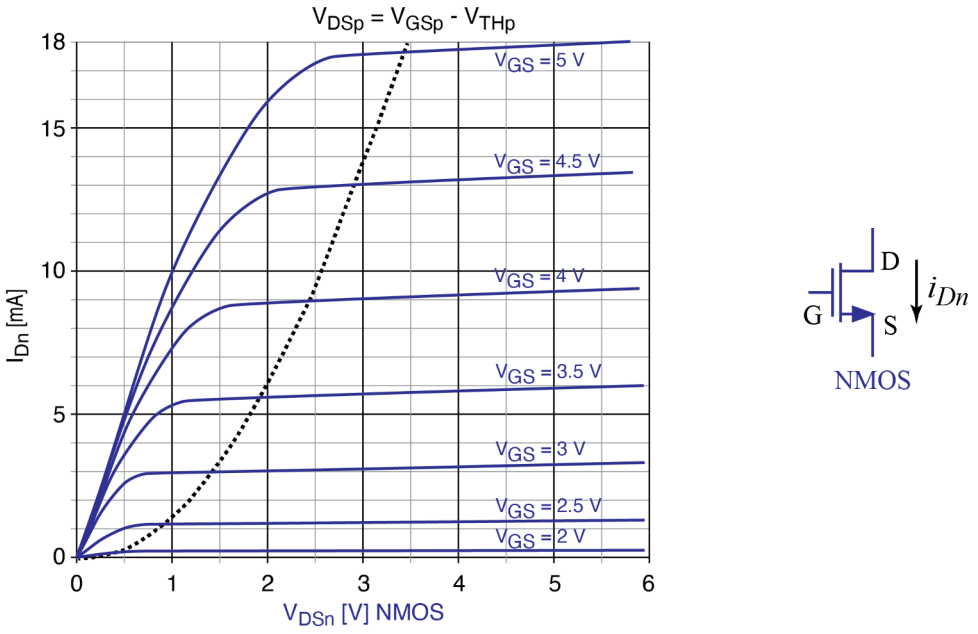


Fig. 4 PMOS characteristic curves redrawn

For the inverter, we overlay the NMOS and PMOS curves, as shown in Fig. 5.

Fig. 4 shows the NMOS FET, which has the same parameters as the PMOS FET ($k_n = k_p$, etc.) but with the signs of I_D, V_{DS}, V_{GS}, and V_{TH} inverted.

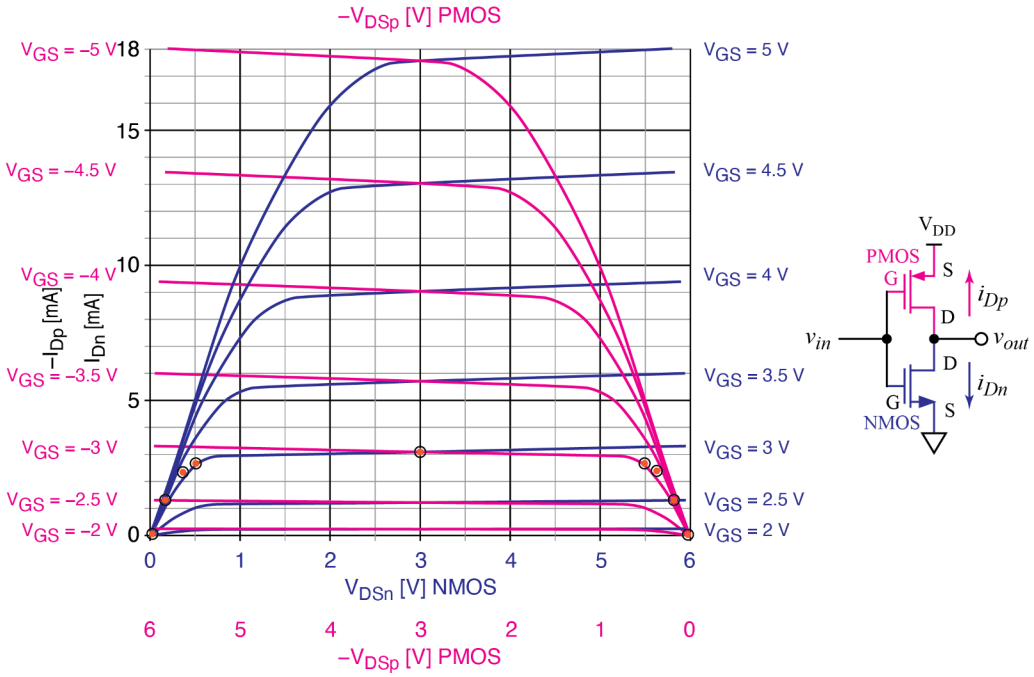


Fig. 5. NMOS and PMOS characteristic curves overlayed for inverter analysis.

Possible operating points shown by circled orange dots.

To determine operating points and the trajectory of voltages and currents when the inverter switches from output high to low, we write a series of constraint equations based on Kirchhoff's laws.

$$V_{DSn} + -V_{DSp} = V_{DD} = 6 \text{ V} \tag{1}$$

$$V_{GSn} + -V_{GSp} = V_{DD} = 6 \text{ V} \tag{2}$$

$$I_{Dn} = -I_{Dp} \tag{3}$$

Fig. 5 shows the possible operating points that satisfy (1)-(3) as orange dots.

When the gate voltage swings from high to low, we see that the current in the inverter is maximum at the midpoint-voltage of 3 V. That maximum current is 3 mA for our example.