

TOOL: Field Effect Transistors (FETs) are used as switches in logic gates to connect the gate output to either the positive voltage source (representing a 1) or to reference (representing a 0). Gate voltages turn the FETs on or off and, since the gates look like small capacitors, the gate current is minimal. The channel between the source and drain acts as a switch controlled by the gate voltage.

NMOS FETs are used as pull down switches and are located at the bottom of the logic gates. PMOS FETs are used as pull up switches and are located at the top of the logic gates. The NMOS FETs turn on when the gate voltage is high relative to the source, which is at a lower voltage. PMOS FETs turn on when the gate voltage is low relative to the source, which is at a higher voltage.

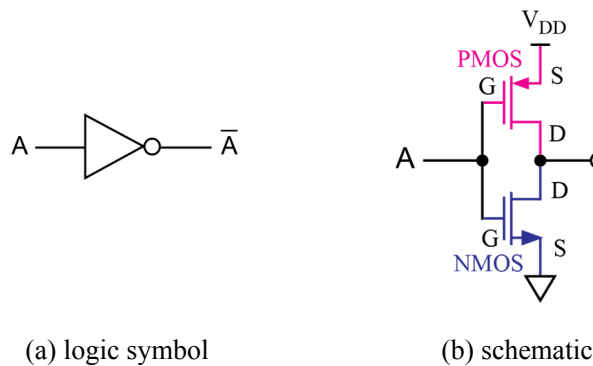


Fig. 1. CMOS inverter.

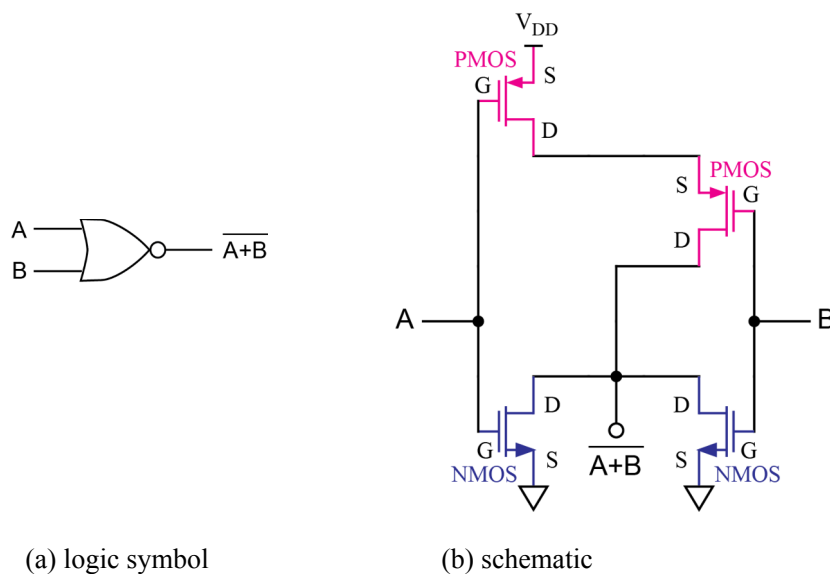


Fig. 2. CMOS NOR gate.

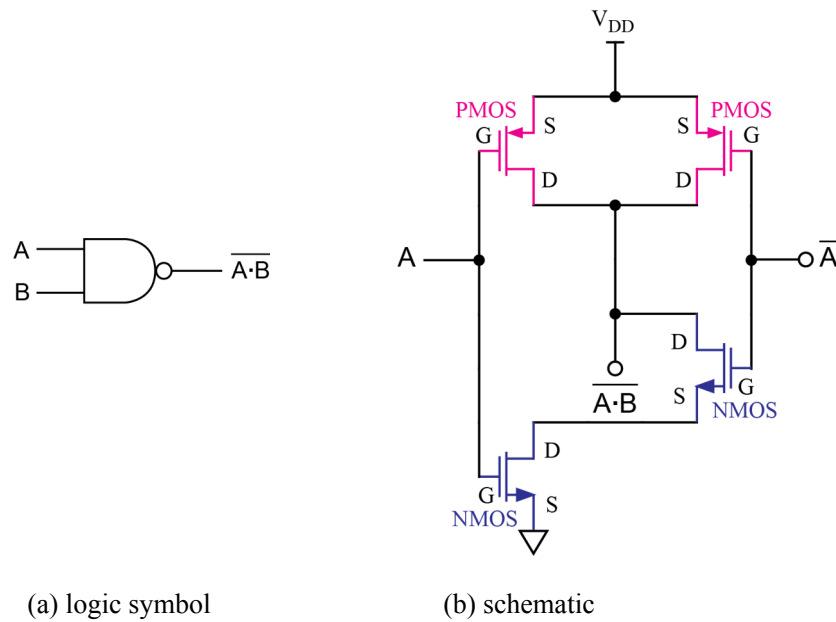


Fig. 3. CMOS NAND gate.